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### C E R T I F I C A T I O N

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Test circuit for the analog measurement of bit line signals of ferroelectric memory cells

This invention relates to a combination of a test circuit with a ferroelectric memory module in accordance with the preamble of patent claim 1. A combination of this type is disclosed in US 5,254,482 A.

Integrated ferroelectric semiconductor memory circuits (FeRAMs) can be constructed in a similar manner to conventional dynamic memories (DRAMs), but differ from the latter through the nonvolatility of the memory content and through differently configured aging phenomena. Tests of the nonvolatility (retention) and of the aging (e.g. fatigue, imprint, disturb,...) therefore require new methods in comparison with DRAM tests. Typical DRAM tests comprise a digital evaluation of the memory content. What is advantageous for the statistical assessment and extrapolation of the decrease in the memory content through stress (for example in the case of electrical or mechanical loading, storage, thermal treatment, irradiation, chemical reactions,...) is, however, an analog evaluation of the memory content through the measurement of analog values of the stored potential. In other words, the analog measurement of bit line signals can already reveal slight stress-induced changes in the potential stored in the cell. This results in substantially more accurate knowledge of the stress influence on the reliability.

In the case of ferroelectric memory modules in development, the path taken heretofore has been to use a special test mode

to indirectly carry out an analog evaluation of the potential stored in the memory cell. As in the case of a DRAM, a customary sense amplifier was used here to compare the bit line signal to be evaluated with a reference signal on a reference bit line. The potential of the reference signal could be adjusted externally. By progressively altering the externally adjustable reference voltage and comparing the two bit line signals with the aid of the sense amplifier, it was possible to obtain a quasi analog information item. However, most of the types of stress could not be evaluated quantitatively using this test method, since the information about the stress influence is lost as early as after the first of the many evaluation cycles required, on account of the destructive read operation of an FeRAM.

Analog information obtained in a test of customary DRAMs has a substantially smaller information content in comparison with a stress test to be carried out in the case of an FeRAM.

In the case of the known combination - described in US 5,254,482 A - of a ferroelectric memory module with a test circuit, the latter is integrated as a ferroelectric capacitor at the edge of a chip having ferroelectric memory modules, and is connected on the one hand to a line that feeds voltage to the ferroelectric memory cells, and on the other hand to a test pad. In this way, said ferroelectric capacitor serves as a dummy memory cell which supplies analog output signals which can be used for extrapolating the aging and fatigue characteristic values of other ferroelectric components in the ferroelectric memory module. In other words, in the case of the known circuit combination, the test circuit does not acquire the genuine signal values - occurring on the bit lines of the ferroelectric memory module - from the ferroelectric memory cells, but instead the signal values that are read out

from the ferroelectric capacitor serving as a dummy cell. This object is achieved as claimed.

It is an object of the invention to specify a cost-effective test circuit for the analog measurement of bit line signals of ferroelectric memory cells with the aid of which the content of ferroelectric memory cells can be read out quantitatively via the potentials on the bit lines and which allows reliable and time-saving evaluation of all stress influences.

According to the invention, a test circuit having one or more analog amplifiers and, in the case of one analog amplifier, a first switching device is accordingly integrated into the ferroelectric memory module, which test circuit, in a test mode with non-activated or disconnected amplifiers, is set up for the analog outputting of bit line signals from the memory module to the outside. Thus, by way of example, analog signals can be tapped off from one or more test pads of the test circuit and be fed for evaluation to a measuring unit which is connected downstream and is connected to the test pad. The output signal to be tapped off at the test pad should represent an unambiguous function of the bit line signal. By way of example it is possible to use one or more analog amplifiers in order to output measurement signals with high resolution. In one embodiment, it is possible to use a separate analog amplifier for each bit line, or alternatively, for example with the aid of a switching device, one analog amplifier for a plurality of bit lines. In the test mode, the sense amplifiers which are used during normal operation are either not activated or are electrically isolated from the bit lines by switching elements.

The test circuit proposed can be fabricated at the same time as the circuit of the memory module in a CMOS basic process without additional process steps.

The test circuit proposed according to the invention has, in particular, the following advantages:

- lower test complexity, shorter test time, lower data processing complexity;
- single-cell evaluation possible with little complexity;
- complete analog information, for example including about retention, possible (in contrast to the previous solution);
- higher resolution, and
- direct outputting of information without loss of information for example through fluctuations of the sense amplifiers.

The above and further features and advantages of a test circuit according to the invention will become even clearer in the description below when the latter is read in relation to the accompanying drawing.

The single figure 1 diagrammatically shows an exemplary embodiment of a test circuit according to the invention and modifications thereof in combination with a ferroelectric memory module which is illustrated diagrammatically and in sections.

The test circuit 1, which is framed by a dashed line, is connected, on the input side, to bit lines  $BL_0$ ,  $\overline{BL_0}$ , ...,  $BL_1$ ,  $\overline{BL_1}$ , ...,  $BL_n$ , and  $\overline{BL_n}$ . During normal operation, these bit lines are connected to sense amplifiers  $LV_0$ ,  $LV_1$ , ...,  $LV_n$  of the ferroelectric memory arrangement. A plurality of memory cells  $Z$  are indicated by large filled-in dots at the crossover points of the bit lines with word lines  $WL_0$ ,  $WL_1$ ,  $WL_2$ ,  $WL_3$ .

For quantitative evaluation of the content of the memory cells Z of the ferroelectric memory arrangement, the test circuit 1 according to the invention passes an analog value of the memory content to the outside via a test pad P. In this way, it is advantageously possible to carry out a statistical assessment and extrapolation of the change in the memory content through stress, as arises through electrical or mechanical loading, storage, thermal treatment, irradiation or through chemical reactions in the ferroelectric memory module. With the aid of the analog values of the memory content, i.e. potentials of the bit line signals, which are measured by the test circuit 1 according to the invention, it is possible to detect even slight stress-induced changes, as a result of which the influences of the stress on the reliability can be accurately assessed. For this purpose, the test circuit 1 according to the invention provides an analog circuit which is integrated in the ferroelectric memory module and, in the exemplary embodiment illustrated, has in each case an analog amplifier A01, A02, A11, A12, ..., An1 and An2 per connected bit line BL, a first switching device S1 and a second switching device S2. The bit lines BL connected to the test circuit 1 can be connected to the inputs of the respective analog amplifiers via the first switching device S1, and the outputs of the analog amplifiers can be fed to a test pad P via the second switching device S2. The first switching device S1 may have individual transistor switches, for example, while the second switching device S2 may be a decoder, for example. An input of a measuring unit M can be connected to the test pad P.

The measuring unit M outputs a test mode signal TM via a line shown dash-dotted, with which signal, during the test mode, the sense amplifiers LV0, LV1, ..., LVn that are connected to the memory cells Z or bit lines BL during normal operation are

deactivated or electrically isolated from the bit lines by further switching elements (not illustrated). The test mode signal TM transmitted by the test unit M also activates a switch controller (not illustrated) which controls the switches of the first switching device S1 and of the second switching device S2 in a targeted manner or in a selectable cycle.

Two alternatives of the test circuit 1 according to the invention are indicated in figure 1. Either an analog amplifier can be used for each bit line BL, or with the aid of corresponding switching elements, a plurality of bit line signals can be fed to inputs of a common analog amplifier A01, A02, as is indicated by dash-dotted lines 11, 12.

The analog amplifiers used in the test circuit 1 according to the invention and, of course, also the switching elements used for the first and second switching devices S1 and S2 are set up in such a way that the measuring unit M can tap off at the test pad P an unambiguous function of the bit line signals. Consequently, the analog values of the memory content which are present on the bit lines BL0,  $\overline{BL0}$ , ..., BL1,  $\overline{BL1}$ , ..., BLn, and  $\overline{BLn}$  in each case represent an unambiguous information item - which can be measured by the measuring unit M - for the contents of the cell respectively addressed, so that the measuring unit M can measure even slight changes in the memory content, caused by stress for example, on the basis of the analog signal which can be tapped off at the test pad P.

It is readily apparent to the relevant persons skilled in the art that the exemplary embodiment of the test circuit according to the invention which can be seen in figure 1 merely represents a basic circuit diagram, and that known evaluation devices and algorithms for evaluating the stress-

induced change in the bit line signals, which reside in the measuring unit M, are not illustrated. Instead of one test pad P, it is also possible to provide a plurality of test pads to which are passed the analog signals from bit lines which are combined in groups by the first and second switching devices and corresponding analog amplifiers.

The analog acquisition of the memory content on the basis of the analog signals fed to the test pad P, which acquisition is proposed according to the invention and made possible by the test circuit 1 described, brings about in particular:

- a lower test complexity, a shorter test time and a lower data processing complexity,
- an evaluation of individual memory cells with little complexity,
- complete analog information assessment of the memory content, for example including changes in said memory content which are brought about by retention,
- a higher resolution, and
- direct acquisition of information without loss of information for example through fluctuations of the sense amplifiers.

Patent Claims

1. A combination of a test circuit with a ferroelectric memory module having a plurality of ferroelectric memory cells (Z), bit lines (BL0,...BLn) and sense amplifiers (LV0,...LVn) connected to the bit lines, the test circuit (1) being integrated in the ferroelectric memory module, characterized

in that the test circuit (1) has either

- in each case an analog amplifier (A01,...AN1, AN2) connected, on the input side, to an associated bit line (BL0,...BLn) of the ferroelectric memory module, or an individual analog amplifier (e.g. A01) for a plurality of bit lines (BL0,...BLn) and a first switching device (S1), in order to connect analog signals from a plurality of bit lines (BL0,...BLn) progressively to an input of the one analog amplifier (e.g. A01),

in which case the test circuit, in a test mode with non-activated or disconnected sense amplifiers (LV0, LVn) of the ferroelectric memory module, outputs the analog signal values occurring on the bit lines from the ferroelectric memory cells connected to the bit lines via the analog amplifier or amplifiers (A01; A01,...AN1) to a point outside the memory module, in order to feed these analog signals to a downstream evaluation device.

2. The combination as claimed in claim 1, characterized in that an output of the test circuit (1) or the output or the outputs of the analog amplifier or amplifiers (A01; A01...AN1) is or are connected to a test pad (P) of the memory module.

3. The combination as claimed in claim 1 or 2, characterized in that a second switching device (S2) is provided at the output of the analog test circuit (1) or of the analog

amplifier or amplifiers (A01; A01,...AN1), with which the analog output signal can be switched from this output or these outputs to an output terminal or a test pad of the memory module.

4. The combination as claimed in one of the preceding claims, characterized in that the test circuit (1) or the analog amplifier or amplifiers (A01; A01,...AN1) is or are set up in such a way that the analog bit line signals to be output can be output with high resolution and without influencing the bit line potentials at the output terminal or test pad (P).

5. The combination as claimed in one of the preceding claims characterized in that the test circuit in the ferroelectric memory module is fabricated at the same time as the circuit of the memory module in a CMOS basic process.



List of reference symbols

A01, A02, A11, A12, ..., An1, An2	Analog amplifiers
BL0, <u>BL0</u> , ..., BL1, <u>BL1</u> , ..., BLn,	
<u>BLn</u>	Bit lines
LV0, LV1, ..., LVn	Sense amplifiers
L1, L2	Multiple line
M	Measuring unit
P	Test pad
S1	First switching device
S2	Second switching device
TM	Test mode signal
WL0, WL1, WL2, WL3	Word line
Z	Memory cell